

FIGURE 1

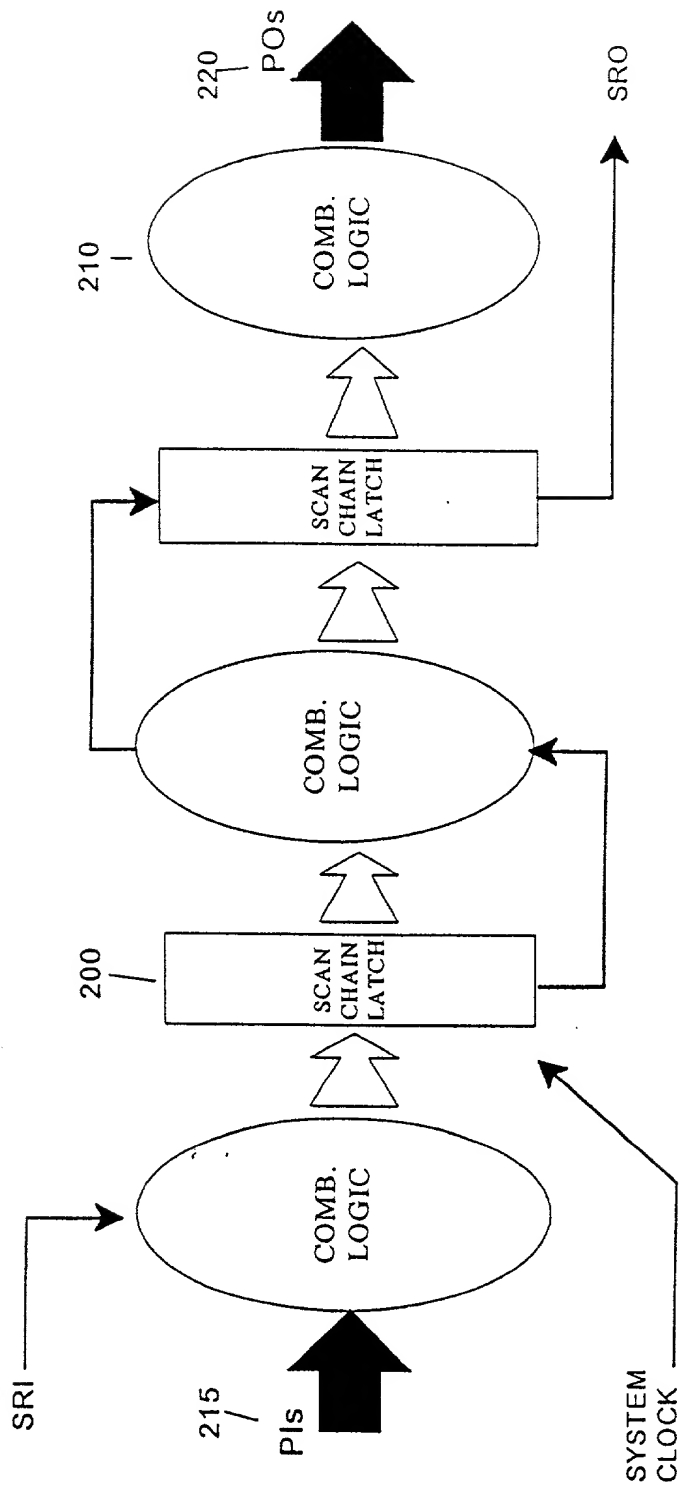


FIGURE 2
PRIOR ART

FIG. 2A is a block diagram of a prior art system 200. The system 200 includes a series of scan registers (SRL₁, SRL₂, SRL₃, ..., SRL_n) connected in a chain. Each scan register SRL_i contains a scan input (SCAN), a scan output (SRO), and a data output (DATA). The scan input of SRL₁ is connected to a scan input signal (SRI) 230. The scan output of SRL₁ is connected to the scan input of SRL₂, and so on. The data output of each SRL_i is connected to a common data output line (DCLK). The scan input of SRL_n is connected to a scan output signal (SRO) 235. The system 200 is controlled by a clock signal (CLK) and a data output clock signal (DCLK).

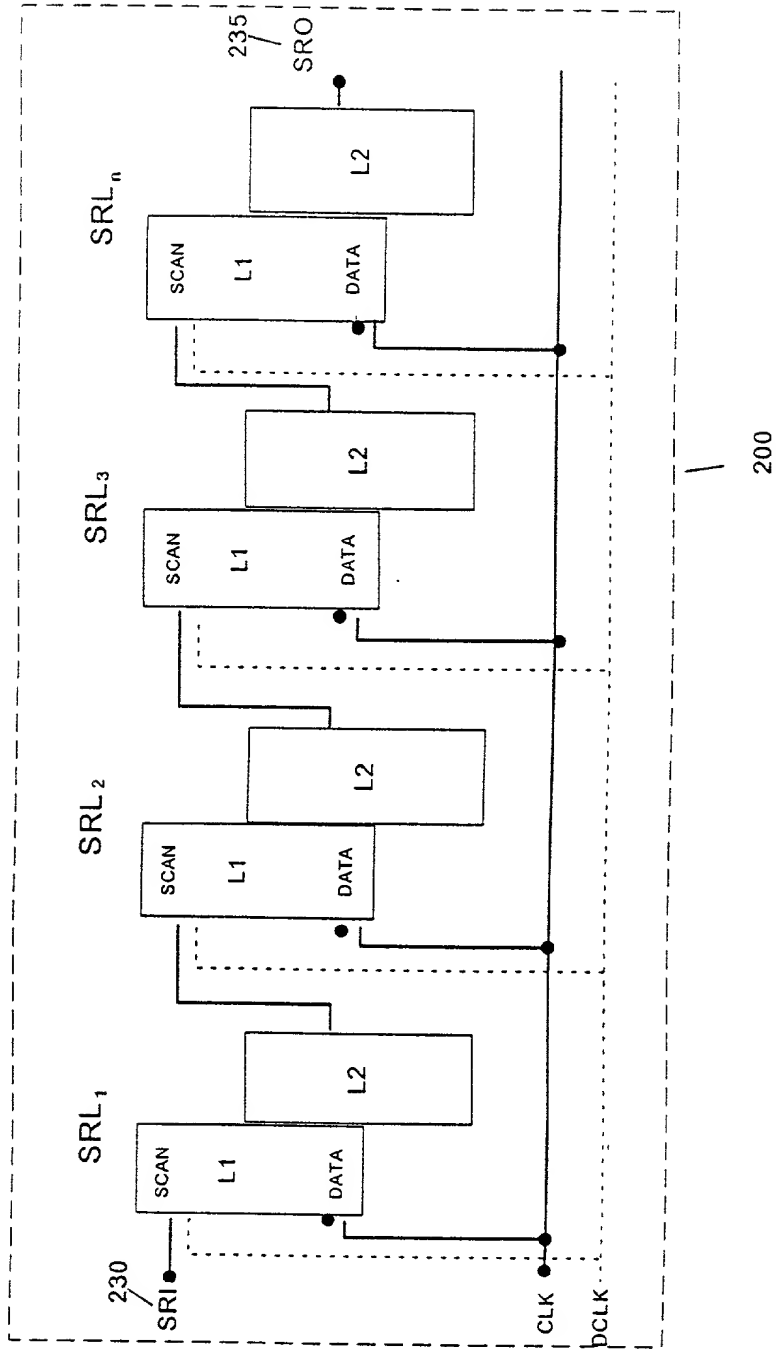


FIGURE 2A
PRIOR ART

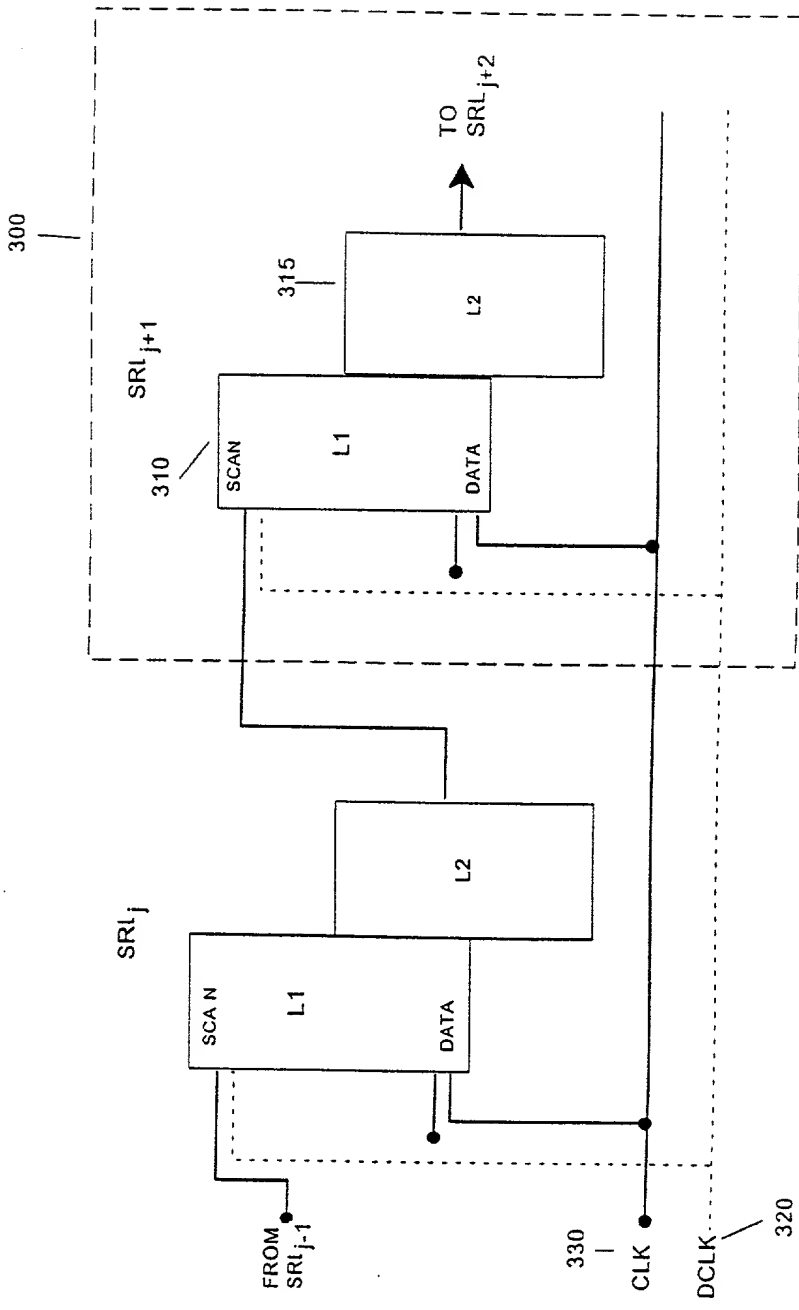


FIGURE 3
PRIOR ART

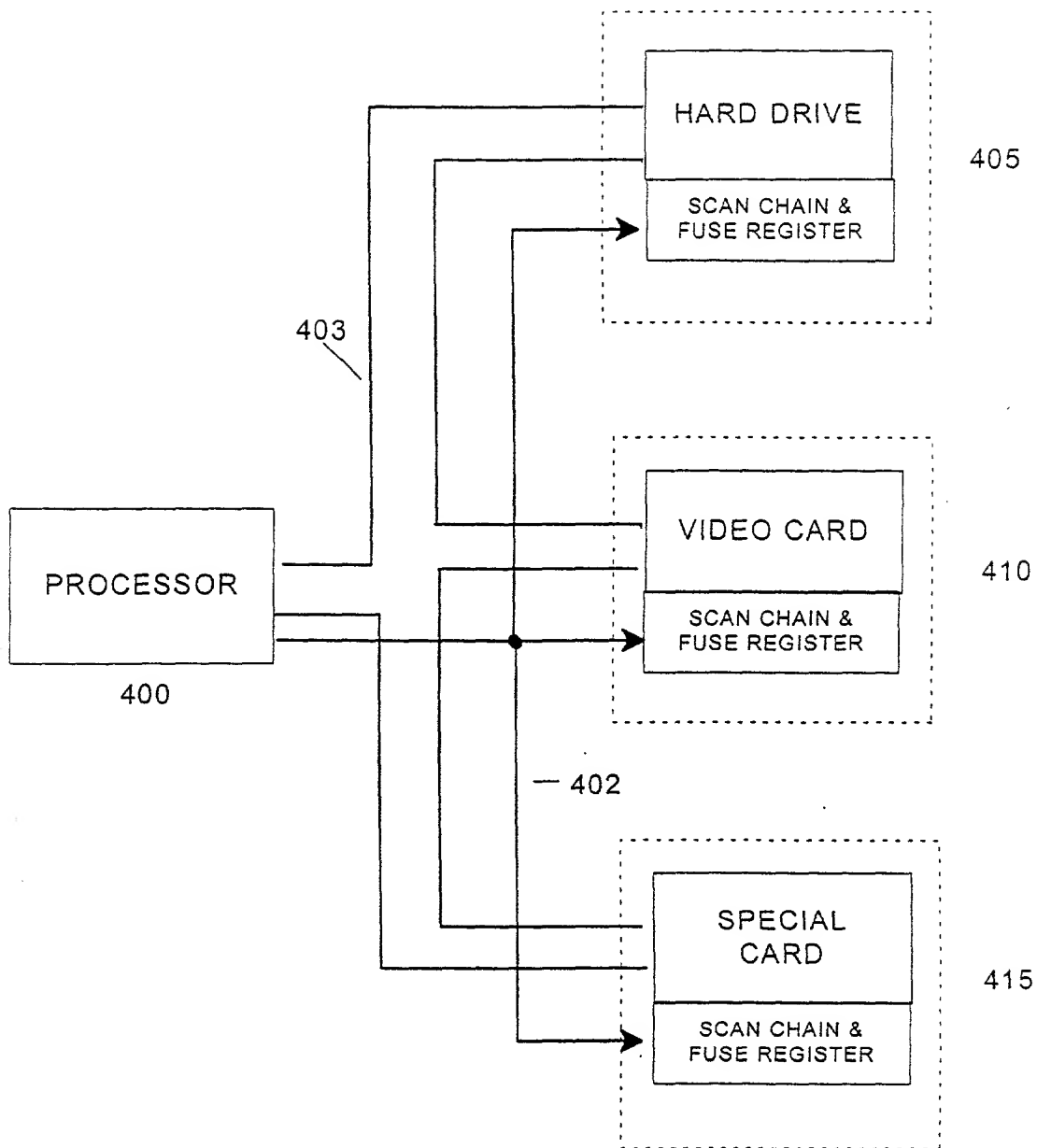


FIGURE 4

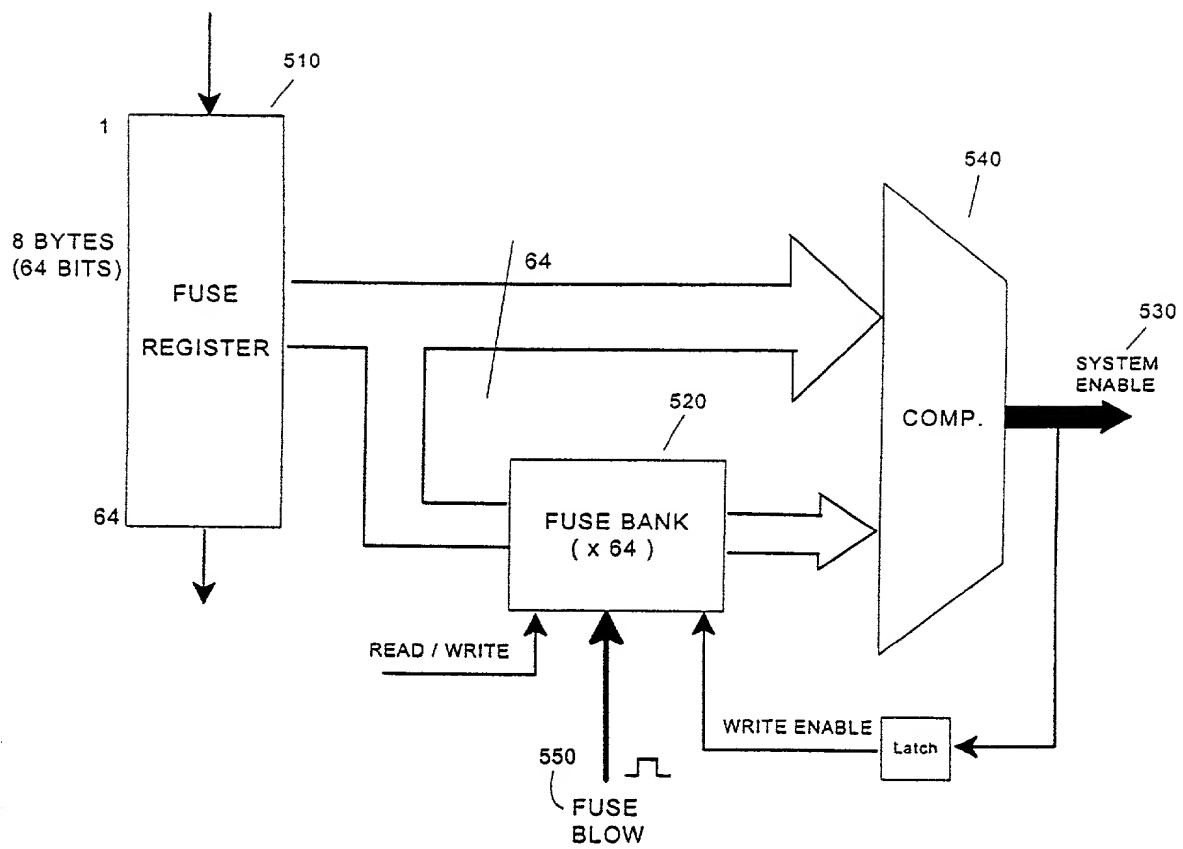


FIGURE 5

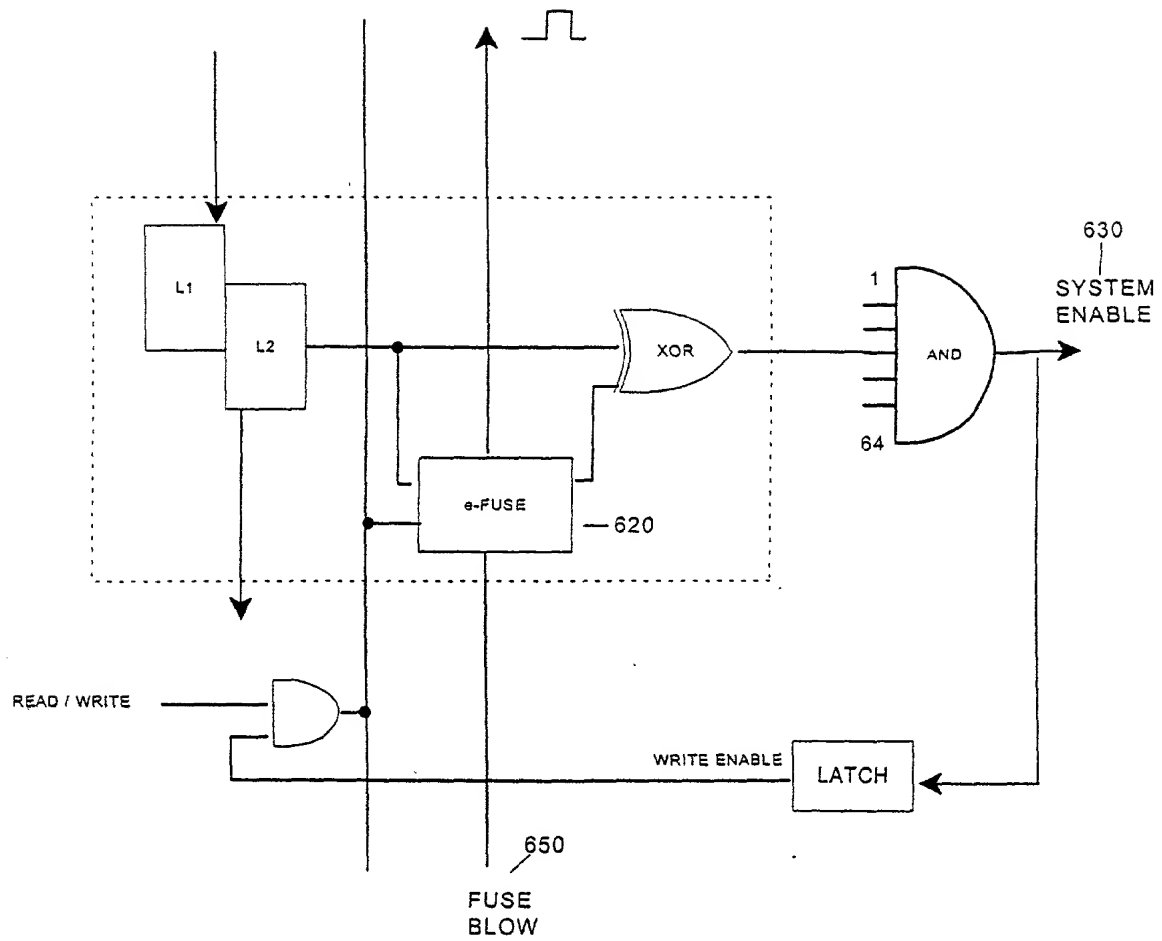


FIGURE 6

SCAN CHAIN GATING

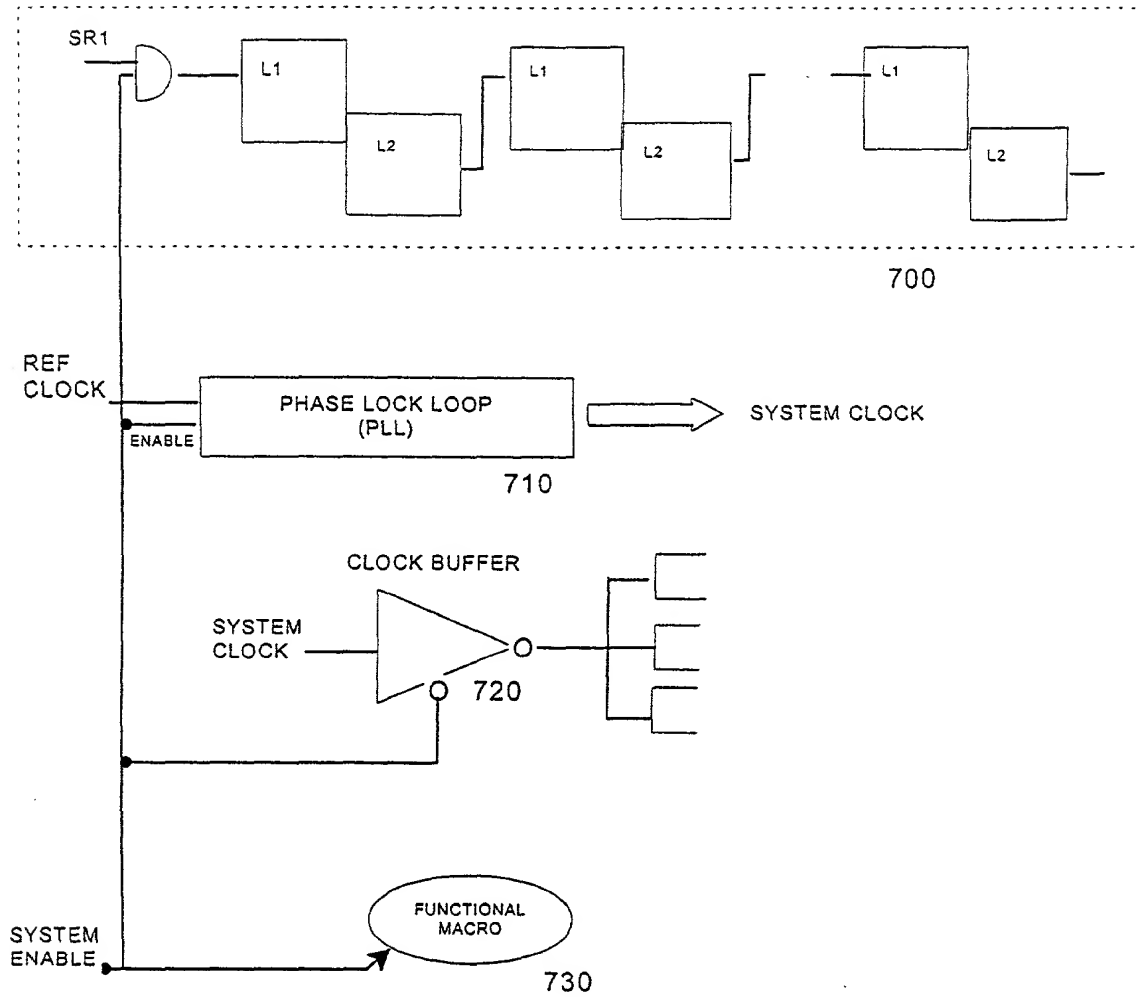


FIGURE 7